Test Report V1.0
Single Event Effects (SEE) Proton Testing of the FM22L16 Ferroelectric Random Access Memory (FRAM)

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I. Introduction

The FM22L16 is an FRAM chip in a configuration of 262,144 x 16 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. Unlike SRAM, the FM22L16 is able to retain data without back-up battery. The memory cells used for the FM22L16 have improved times of read/write access per bit, significantly outperforming FLASH memory and EEPROM in durability. The FM22L16 uses a pseudo - SRAM interface compatible with a JEDEC 256Kx16 SRAM pin out. The FRAM was tested at Indiana University Cyclotron Facility (IUCF).

II. Devices Tested

The FRAM devices were designed and fabricated by Ramtron International Corporation. They are fabricated in the advanced high-reliability ferroelectric process. All devices were characterized prior to exposure. The five devices tested are from the 0645 Lot Date Code (LDC). Complete package markings for the devices are:

FM22L16
6104400
Normal
0645

These are all 44 pin devices in a TSOP-II package. The devices, de-lid at NASA GSFC, are shown in the before and after pictures below.

Product Datasheet: http://www.tecnikadue.it/file/1609.pdf

Figure 1: Pictures of the FRAM device package.

III. Test Facility

Facility: Indiana University Cyclotron Facility

Total Beam Time: 8 hours

Flux: 4.55×10^7 to 2.78×10^8 p/cm^2/s

Minimum fluence achieved per part: 1.12×10^{11} p/cm^2

Proton Energies: 198MeV, 140MeV, 89MeV

IV. Test Methods

Temperature: Room temperature

Test Voltage: Nominal (3.3 Volts), high (3.6 Volts), and low (3.0 Volts)

Operating Frequency: Nominal operating frequency

Test Hardware:

The Low Cost Digital Tester (LCDT) was used to perform this testing. A device under test (DUT) socketed daughter card was developed and the appropriate VHDL written to the LCDT in order to perform the required SEE testing as detailed below. Appropriate power supplies were used with DUT current strip charted and monitored for over current conditions. Figure 2 depicts the test setup.

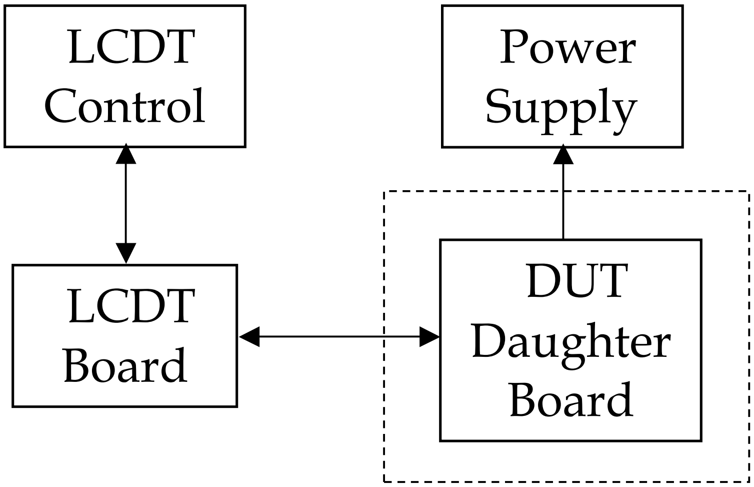
LCDT Control
Power Supply
LCDT Board
DUT Daughter Board

Figure 2: Block Diagram of test setup, where the dashed line represents the component within the beam path

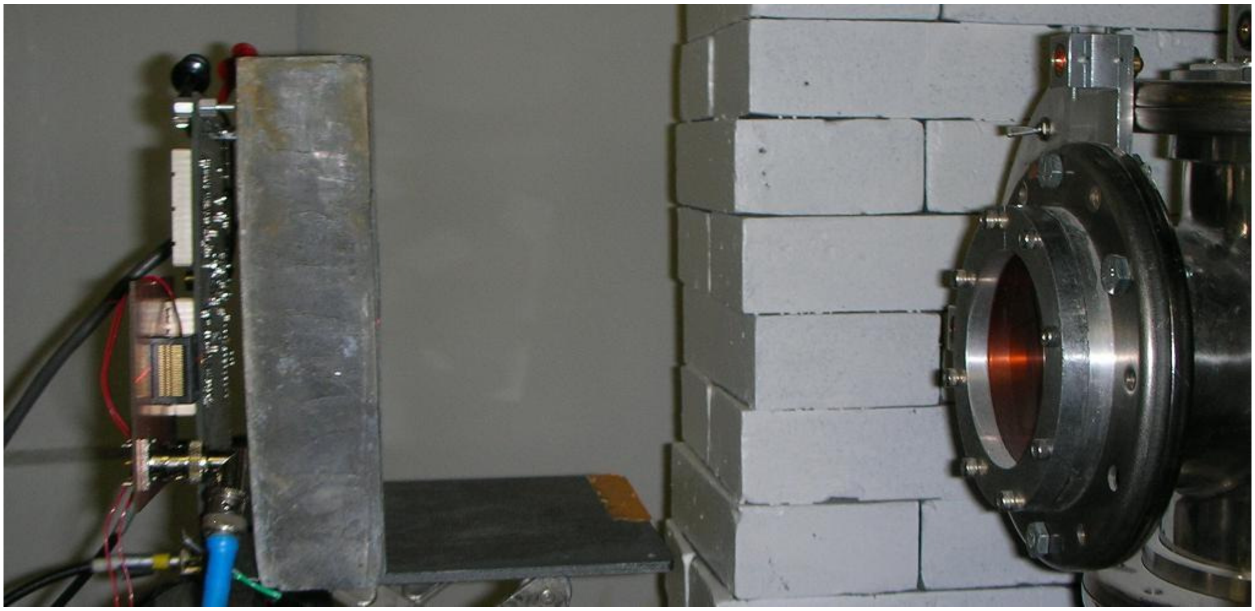

Figure 3: Photo of the device setup in the beam path

Procedure:

Prior to exposure a test pattern was written to the memory cells, a checkerboard of zeroes and ones. Then the test was run dynamically (read continuously during beam exposure) until a desired fluence was met.

V. Test Results

Expected Single Event Errors (SEE):

Single Event Upset (SEU) – Single and/or multi-bit errors, as well as multi-cell errors when the memory is read. A known pattern is written and expected when read; any variation from the known pattern will show this type of SEE.

Single Event Functional Interrupt (SEFI) – Unexpected mode changes, test modes, halt, pointer errors, etc. This type of SEE can be observed if excessive errors remain after the part is power cycled and/or reset.

Single Event Latchup (SEL) – Latchup, an electrical condition, may occur if the internal resistance of a part's region allowing for over current conditions to occur. This type of SEE can be seen in the supply current value exceeding the maximum current described in the part's datasheet.

Results Observed:

Dynamic Errors – summation, over all *dynamic* tests, of addresses where unexpected values were repeatedly read from the memory cells *during* beam exposure. Expected values were that of the pattern written before test run. The memory cells were read continuously until a desired fluence was met, and the actual amount of corrupt cells at the end of the test was further investigated, considered a SEU.

Stuck Bit Errors – Memory cells reported as still in error after the device has been read for errors and rewritten, considered a SEFI.

Testing:

Five FRAM parts were tested in the IUCF proton beam; all were tested in dynamic mode, for proton energies of 198MeV and 140MeV. Two of which were also tested at a proton energy of 89MeV, to obtain the following results:

Occurrence:	Energy where events were observed:
Dynamic Errors:	Observed at all energies
Stuck Bits:	Observed at all energies

Table 1: Energy extremities of events

No more than 10% of the memory cells upset during any one run. No pattern sensitivity was shown in the testing that was conducted.

DUT Number:	157	170	174	176	177
Test Voltages (V):	3.0, 3.6	3.0, 3.6	3.3	3.3	3.3
Number of runs:	6	9	8	4	5
Temperature:	75C	75C	Room Temp.	Room Temp.	Room Temp.
Total Fluence:	1.12E11	1.30E11	2.90E11	2.00E11	3.00E11
Dynamic Errors:	3	12	283	180	780
Runs with stuck bits:	1	0	2	2	1
Total Dose to part (kRad):	7.487	7.792	23.32	13.51	23.92
Comments	More data needed for statistics	n/a	n/a	n/a	n/a

Table 2: Detailed results for DUTs

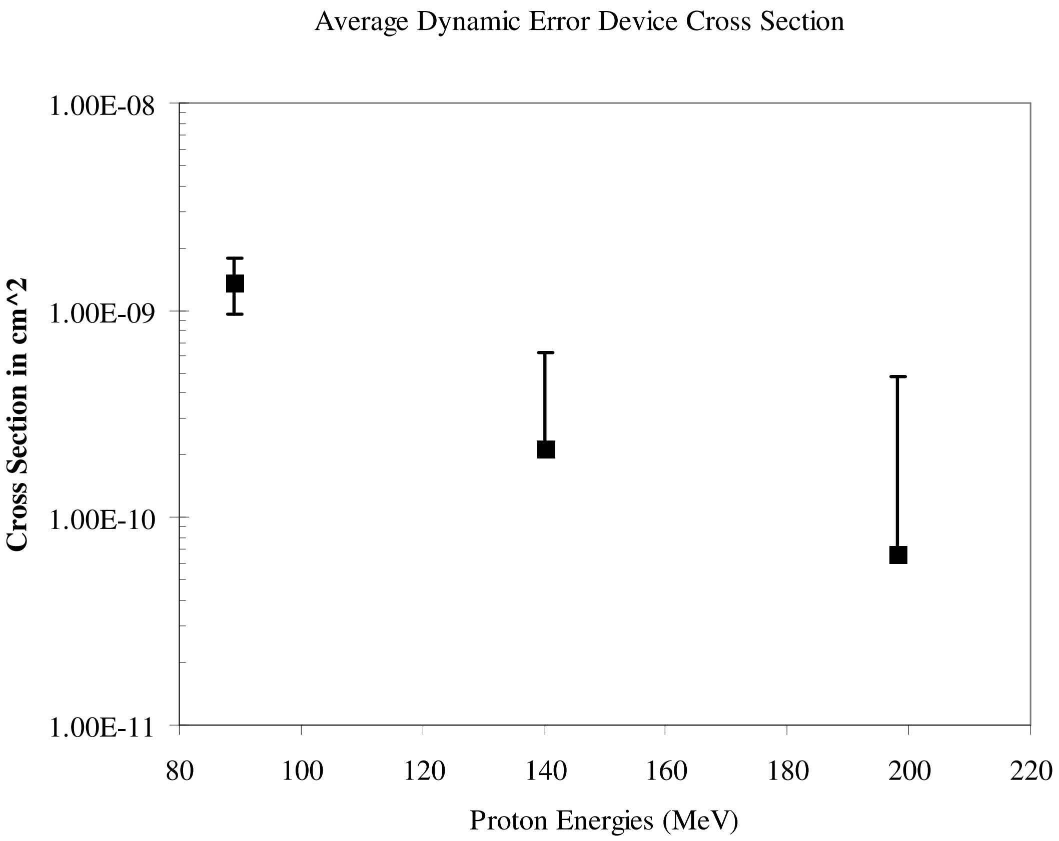

Figure 4: Device Cross Section

SEL Investigation:

The devices numbered 157 and 170 were both tested at elevated temperature and high source voltage for latch-up conditions. No SEL was recorded at the energies tested.

Test Requirements Met:

1. Testing is to be conducted at nominal (3.3 Volts), high (3.6 Volts), and low (3.0 Volts) voltages.
2. FRAM test pattern was controllable with a minimum requirement of an all zeros, all ones, checkerboard and reverse checkerboard patterns.
3. Testing was done in the dynamic mode.
4. Testing was done over 3 proton energies obtaining a statistically significant amount of errors.

Test Requirements Not Met:

1. Testing was not done for all ones and all zeroes pattern.
2. Testing was not extensive enough to determine susceptibility to SEL.